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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,191	05/20/2004	Tsukasa Shiraishi	2004-0787	7292

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EXAMINER


WILLIAMS, ALEXANDER O

ART UNIT PAPER NUMBER

2826

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/849,191	<b>Applicant(s)</b> SHIRAISHI ET AL.	
	<b>Examiner</b> Alexander O. Williams	<b>Art Unit</b> 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 October 2005.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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Serial Number: 10/849191 Attorney's Docket #: 2004\_0787

Filing Date: 5/20/2004; claimed foreign priority to 11/29/2000

Applicant: Shiraishi et al.

Examiner: Alexander Williams

Applicant's Request for Reconsideration filed 10/26/05 to the election without traverse of species figure 6 (claims 1 to 3), filed 5/12/05, has been acknowledged.

Acknowledgment is made for applicant's translation of claim for foreign priority under 35 U.S.C. 119(a)-(d) certified copy filed 10/26/05.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Papageorge et al. (U.S. Patent # 5,438,224.

1. Papageorge et al. (figures 1 to 7) specifically figures 1 to 3 and 6 show a semiconductor device module 100 comprising: a semiconductor device including: a multi-layer wiring board 130 which comprises insulation layers 132,134 and circuit pattern layers 139, laminated alternately and is provided with a three-dimensional wiring comprising said circuit pattern layers provided on both sides of the insulation layer and a plurality of inner via holes 135 penetrating through each of said

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insulation layers and electrically connecting; at least a first semiconductor element 120 mounted on the one side of the multi-layer wiring board and a second semiconductor element 110 mounted on the other side of said multi-layer wiring board wherein electrodes of said semiconductor elements are connected with each other by means of said three-dimensional wiring; and a mother multi-layer wiring board 150 having a circuit pattern formed on said surface thereof, wherein said semiconductor device is mounted on said mother multi-layer wiring board and said semiconductor device and said mother multi-layer wiring board are connected by electrical connection means 152,410.

2. The module of the semiconductor device according to claim 1, Papageorge et al. show wherein said electrical connection means 152,410 is a projecting electrode which is interposed between said multi-layer wiring board of said semiconductor device and said mother multi-layer wiring board by bonding said back surface of said second semiconductor element onto said mother multi-layer wiring board thus placing said semiconductor device on said mother multi-layer wiring board, thereby to connect said circuit pattern provided on said multi-layer wiring board and said circuit pattern provided on said mother multi-layer wiring board.

3. The module of the semiconductor device according to claim 1, Papageorge et al. show wherein said electrical connection means 152,410 is an electrically conductive supporting body which is electrically connected to said wiring in said multi-layer wiring board of said semiconductor device and is also used to fasten said semiconductor device onto said mother multi-layer wiring

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board, so as to establish electrical connection between said wiring of said multi-layer wiring board of said semiconductor device and said circuit pattern provided on said mother multi-layer wiring board by fastening said semiconductor device onto said mother multi-layer wiring board via said electrically conductive supporting body.

## Response

Applicant's arguments filed 10/26/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,778,734,668,779,700,701,758,691,6 98,E25.013,E23.114, 361/767,768,803,818,792,760,763,782,784,794,795	7/21/05 12/29/05
Other Documentation: foreign patents and literature in 257/686,685,723,777,778,734,668,779,700,701,758,691,6 98,E25.013,E23.114, 361/767,768,803,818,792,760,763,782,784,794,795	7/21/05 12/29/05
Electronic data base(s): U.S. Patents EAST	7/21/05 12/29/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams  
Primary Examiner  
Art Unit 2826

AOW  
12/29/05